UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/038,613	01/08/2002	Toru Iwata	60188-137	7765

7590 10/18/2005

Jack Q. Lever, Jr.
McDERMOTT, WILL & EMERY
600 Thirteenth Street, N.W.
Washington, DC 20005-3096

EXAMINER	
GHULAMALI, QUTBUDDIN	
ART UNIT	**PAPER NUMBER**
2637	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/038,613	IWATA ET AL.	
	Examiner	Art Unit	
	Qutub Ghulamali	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 10-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-12* is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to the Amendment filed by the applicant on 07/25/2005.

2. Amendment of claims 1, 2, 7, and 10, and cancellation of claim 9, filed by the applicant on 07/25/2005, is hereby acknowledged.

3. The applicant's amendment of claims 1, 2, and 7, however, does not place the claims in condition for allowance, and rejection to claims 1-8, is therefore, maintained.

4. In view of applicant's amendment of claim 7, the rejection to 35 U.S.C. 112, second paragraph is hereby withdrawn.

Response to Arguments/Amendments

5. Applicant's arguments/amendments, filed 07/25/2005, regarding claims 1, 2, and 7, has been considered but does not place the application in condition for allowance.

The applicant's Remarks/Arguments, pages 7-10, regarding amended claims 1, 2, and 7, have been fully considered but are not persuasive.

With reference to claim 1, the applicant asserts that Aoki (696) fails to disclose duty factor controller for adjusting a data transition characteristics (transitions) converted phase value of a received pilot signal.

Examiner's response – The examiner disagrees. The examiner respectfully would like to draw applicant's attention to specific areas by Aoki that enumerating applicants claimed subject matter. Aoki (figs 2, 4, 7, 8, 24, 25) discloses a duty judging circuit (fig. 7, element 8 and fig. 8,

element 9) in conjunction with data selector 9, wherein the duty judging circuit in fig. 7 is composed of duty calculation section 1101 and a flip-flop circuit 1107 to store the phase sampled data in shift register 1102, the duty calculation circuit 1101 calculates the lengths of "1" and "0" to produce a duty ratio (adjustment) of the input data as the duty information at 109 to conditioning judging circuit 1301 which is in turn is composed of an edge counter 1302 that count edges based on sample data to produce phase selection information S1303 in case of error between two edges of sampled data within one cycle (col. 4, lines 41-49; col. 7, lines 29-40, 49-54, 56-67; col. 8, lines 1-4; col. 11, lines 27-35). Based on disclosed information by Aoki, the examiner firmly believes that Aoki clearly shows the claimed limitation "duty factor controller for adjusting a data transition characteristics (transitions) converted phase value of a received pilot signal". The claim rejection is, therefore, maintained.

As per applicant's remarks regarding Aoki-Engdahl combination with reference to rejection of claim 2, the examiners offers the following response: When an obvious determination or motivation to combine two or more references, there must be some suggestion or motivation to combine the references. See In re Rouffet, 149 F. 3d 1350, 1355, 47 USPQ 2d 1453, 1456 (Fed. Cir. 1998). The suggestion to combine may be found in explicit or implicit teachings within the reference themselves, from the ordinary knowledge of those skilled in the art, or from the nature of the problem to be solved. See id. At 1357, 47 USPQ 2d at 1458. Moreover, as long as some motivation or suggestion to combine the references is provided by the prior art taken as a whole, the law does not require that the references be combined for reasons contemplated by the inventor. See In re Dillon, 919 F. 2d 688, 693, 16 USPQ 2d 1897, 1901 (Fed. Cir. 1990) (en banc), cert. Denied, 500 U.S. 904 (1991) and iIn re Beattie, 974 F. 2d 1309,

1312, 24 USPQ 2d 1040, 1042 (Fed. Cir. 1992). Thus, as stated by the examiner, the advantages described by Engdahl would have motivated one of ordinary skill in the art to employ a driver for supplying a differential data in the clock recovery circuit of Aoki.

As per claim 7, applicant indicates that Miyashita is silent to "a means for controlling a transition characteristic of the data signal". The examiners response - The examiner respectfully would like to draw applicant's attention to Miyashita (828), disclose in the abstract and in col. 2 lines 51-67 and col. 3, lines 1-4 in the clock reproduction circuit, the frequency error detection circuit detects the frequency difference between the data clock and the VCO clock by detecting the phases of the VCO clock at transition edges (characteristics) of the data signal and by detecting changes in the detected phases thereby the frequency difference between the data clock and the VCO clock can be detected by detecting a change in the phases of the VCO clock at the transition edges. Miyashita, similarly, further discloses very clearly the claimed limitations in col. 3, lines 10-25; wherein a means for controlling a transition is provided via the detection/hold circuits each of which detects a phase of the clock at one transition edge, holds the detected phase and cancels the held value. The examiner therefore believes Aoki very clearly discloses the embodiments of the claimed invention, and therefore, the rejection to claim 7 is still maintained.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al (US Patent 6,236,696) in view of Engdahl et al (US Patent 5,493,571).

Regarding claim 1, Aoki discloses a clock recovery circuit in which a timing jitter (error) in a recovered clock is suppressed (reduced, minimized), the clock recovery circuit comprising:
a duty factor controller for adjusting a data transition characteristic of the transceiver means so as to reduce a duty factor error in a data signal supplied from the transceiver means in the first period, and having the adjusted data transition characteristic stored (col. 11, lines 16-35; col. 12, lines 15-20, 35-40); and
a clock recovery unit for recovering, from the data signal supplied from the transceiver means, a clock synchronized with the data signal in the second period (col. 26, lines 3-14).
Aoki however, is silent regarding "transceiver means for supplying a data signal, which is based on serial data having a regular bit pattern during a first period, and is based on serial data having an arbitrary bit pattern during a second period following the first period" and "a driver for supplying a differential data; and
a receiver for receiving the differential data signal from the driver and supplying a single end signal corresponding to the differential data signal, wherein a data transition characteristic of the driver or the receiver is adjusted by the duty factor". Engdahl in a similar field of endeavor discloses transceiver for supplying a data signal, which is based on serial data having a regular bit pattern during a first period, and is based on serial data having an arbitrary bit pattern during a second period following the first period (abstract; col. 3, lines 16-25, 30-67; col. 5, lines 48-52,

60-67; col. 6, lines 10-17), and a driver for supplying a differential data (col. 20, lines 56-61); and

a receiver for receiving the differential data signal from the driver and supplying a single end signal corresponding to the differential data signal, wherein a data transition characteristic of the driver or the receiver is adjusted by the duty factor (col. 20, lines 60-67; col. 21, lines 1-8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use transceiver to supply data signal having a regular bit pattern (preamble) during a first period and an arbitrary (data field) bit pattern during a second period as taught by Engdahl in the clock recovery of Aoki so as to facilitate synchronization of supplied data (bit pattern) to recover the clock.

Regarding claim 2, Aoki discloses all limitation to claim 2 but fails to disclose a driver for supplying a differential data signal and a receiver for receiving the differential data signal. Engdahl in a similar field of endeavor discloses:

the driver supplies a differential data signal to the receiver (col. 20, lines 56-61). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a driver for supplying a differential data signal to receiver circuit as taught by Engdahl in the clock recovery of Aoki because it can allow the duty factor controller to adjust a data transition characteristic of the driver.

8. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al (US Patent 6,236,696) in view of Engdahl et al (US Patent 5,493,571) as applied to claim 1 above, and further in view of Zerbe et al (US Patent 6,643,787).

With reference to claim 3, Aoki in combination with Engdahl discloses all limitations highlighted above, except a duty factor controller includes an integrator circuit for integrating the data signal so as to output an analog voltage representing a duty factor error in the data signal. Zerbe in a similar field of endeavor discloses:

a duty factor controller includes an integrator circuit (figs. 16, 17, element 171) for integrating the data signal so as to output an analog voltage representing a duty factor error in the data signal (col. 13, lines 45-67; col. 14, lines 1-27). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an integrator circuit for integrating the data signal so as to output an analog voltage representing a duty factor error in the data signal as taught by Zerbe in the combined clock recovery circuit of Aoki and Engdahl, so as to facilitate integration of data signal in minimizing duty factor or duty cycle errors as desired.

9. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al (US Patent 6,236,696) and Engdahl et al (US Patent 5,493,571) in view of Zerbe et al (US Patent 6,643,787), as applied to claims 1 and 3 above, and further in view of O'Toole et al (US Patent 6,466,634).

Regarding claim 4, Aoki and Engdahl in combination with Zerbe disclose all limitations to claim 1 and 3 above, except duty factor controller further includes an A/D converter. O'Toole in a similar field of endeavor discloses duty factor an A/D converter (col. 77, lines 34-44; col. 80, lines 14-21) that can easily be implemented in an integrated form for giving the transceiver means a digital signal according to the analog output voltage from the integrator circuit as a duty factor control signal. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use an A/D converter for giving the transceiver means a

digital signal according to the analog output voltage from the integrator circuit as a duty factor control signal as taught by O'Toole in the combined clock recovery circuit of Aoki, Engdahl and Zerbe so as to provide digital signal to the control of duty cycle of the signal.

10. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al (US Patent 6,236,696) in view of Engdahl et al (US Patent 5,493,571) as applied to claim 1 above, and further in view of Zerbe et al (US Patent 6,643,787).

Regarding claim 5, Aoki in combination with Engdahl, discloses all of the claimed limitations, except fails to disclose a delay circuit and a logic circuit. Zerbe in a similar field of endeavor discloses a delay circuit (figs. 7, 40) for generating a delayed data signal that is delayed by one data interval (between with respect to the data signal (col. 8, lines 59-65; col. 26, lines 1-14); and

a logic circuit (registers) for giving the transceiver means a duty factor control signal according to a plurality (performs a sequence of data writes) of logical operation results of the data signal and the delayed data signal (col. 26, lines 5-14). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a delay circuit and a logic circuit as taught by Zerbe in the combined clock recovery circuit of Aoki and Engdahl, because it can allow the communication devices to perform sequence of read write operations to arrive at optimal offset.

Regarding claim 6, Aoki in combination with Engdahl, discloses all of the claimed limitation, except fails to disclose detecting a phase in the clock with respect to the data signal and giving the transceiver means a duty factor control signal according to a magnitude of the phase error. Zerbe in a similar field of endeavor discloses detecting a phase error in the clock

with respect to the data signal and giving the transceiver means a duty factor control signal according to a magnitude (scale) of the phase error (Col. 8, lines 66-67; col. 9, lines 1-13). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include means for detecting phase error in the clock with respect to the data signal and give a control signal as taught by Zerbe in the combined clock recovery circuit of Aoki and Engdahl, because it can provide adjustment capabilities in minimizing errors or offset with the recovered clock.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 7-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Miyashita et al (US Patent 5,889,828).

Regarding claim 7, Miyashita discloses a clock recovery circuit for recovering a clock synchronized with a data signal comprising: a voltage controlled oscillator (912, 961) for generating a clock having a frequency according to a control voltage (col. 10, lines 14-19); first charge pump (965) and a second charge pump (967) whose respective outputs are coupled to a common node (col. 12, lines 37-60);

a first phase detector for detecting a phase error in the clock with respect to one of a rising edge and a falling edge of the data signal so as to control the first charge pump according to the phase error (col. 12, lines 38-67; col. 13, lines 58-67; col. 14, lines 9-35);

a second phase detector for detecting a phase error in the clock with respect to the other one of the rising edge and the falling edge of the data signal so as to control the second charge pump according to the phase error (col. 10, lines 49-67; col. 11, lines 1-25; col. 14, lines 9-61); and

a means for controlling a transition characteristic of the data signal according to an output of one of the first and second phase detectors (col. 3, lines 10-25),

wherein a voltage that is generated at the common node by the first and second charge pumps is given to the voltage controlled oscillator as the control voltage so that the Phase error detected by the first phase detector and the phase error detected by the second phase detector are both reduced (col. 14, lines 9-61).

With reference to claim 8 Miyashita discloses the data signal is a data signal of an NRZ format (col. 9, lines 57-65; col. 10, lines 14-20).

Allowable Subject Matter

13. Claims 10-12 allowed.

Conclusion

14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Qutub Ghulamali whose telephone number is (571) 272-3014. The examiner can normally be reached on Monday-Friday from 8:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QG.
October 16, 2005.

JEAN B. CORRIELUS
PRIMARY EXAMINER
10-17-05